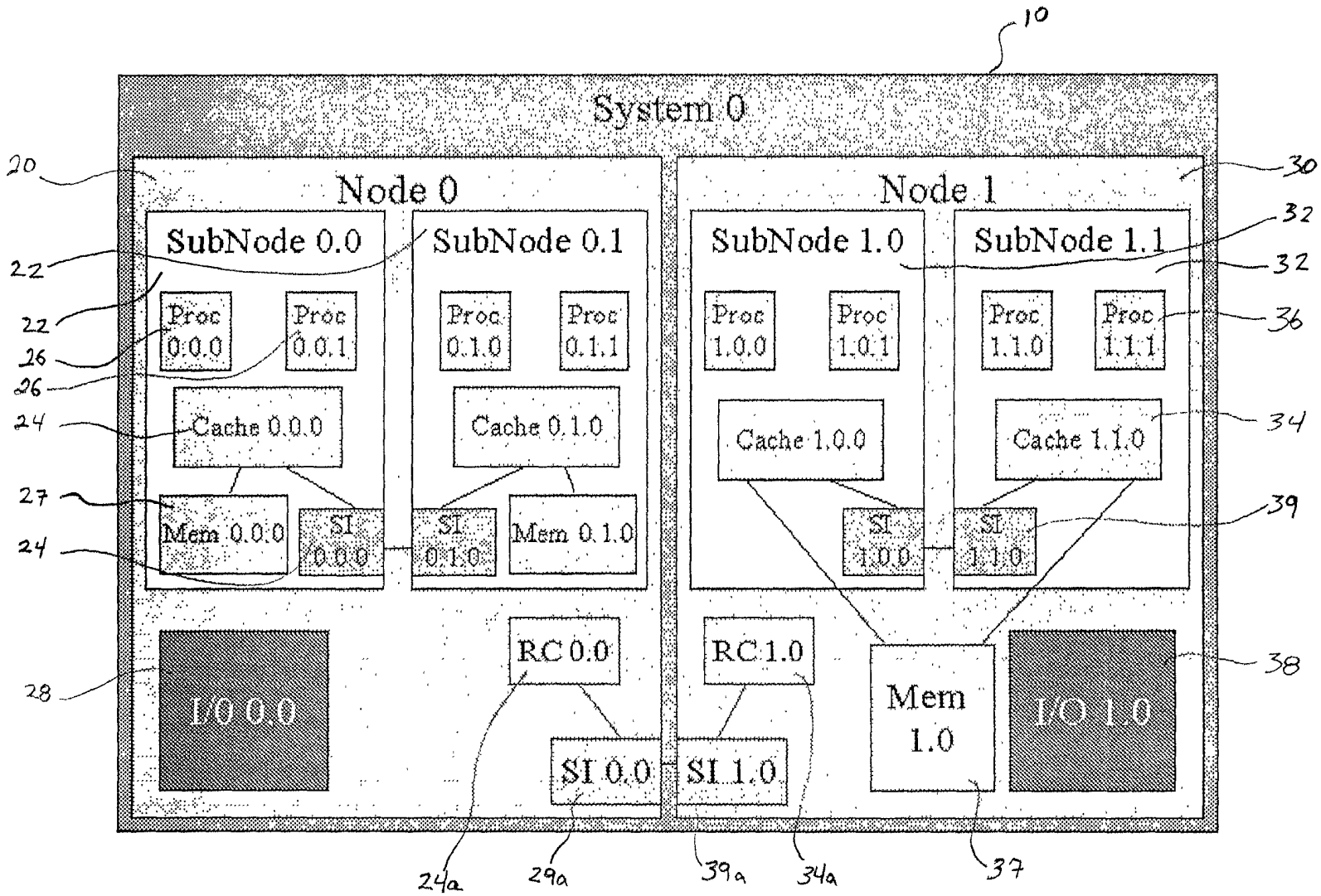

10
System 0
20
Node 0
30
Node 1
SubNode 0.0
SubNode 0.1
SubNode 1.0
SubNode 1.1
32
22
Proc 0.0.0
Proc 0.0.1
Proc 0.1.0
Proc 0.1.1
Proc 1.0.0
Proc 1.0.1
Proc 1.1.0
Proc 1.1.1
36
26
Cache 0.0.0
Cache 0.1.0
Cache 1.0.0
Cache 1.1.0
34
24
27
Mem 0.0.0
SI 0.0.0
SI 0.1.0
Mem 0.1.0
SI 1.0.0
SI 1.1.0
39
RC 0.0
RC 1.0
28
I/O 0.0
Mem 1.0
I/O 1.0
38
SI 0.0
SI 1.0
24a
29a
39a
34a
37

FIG. 1

FIG. 2

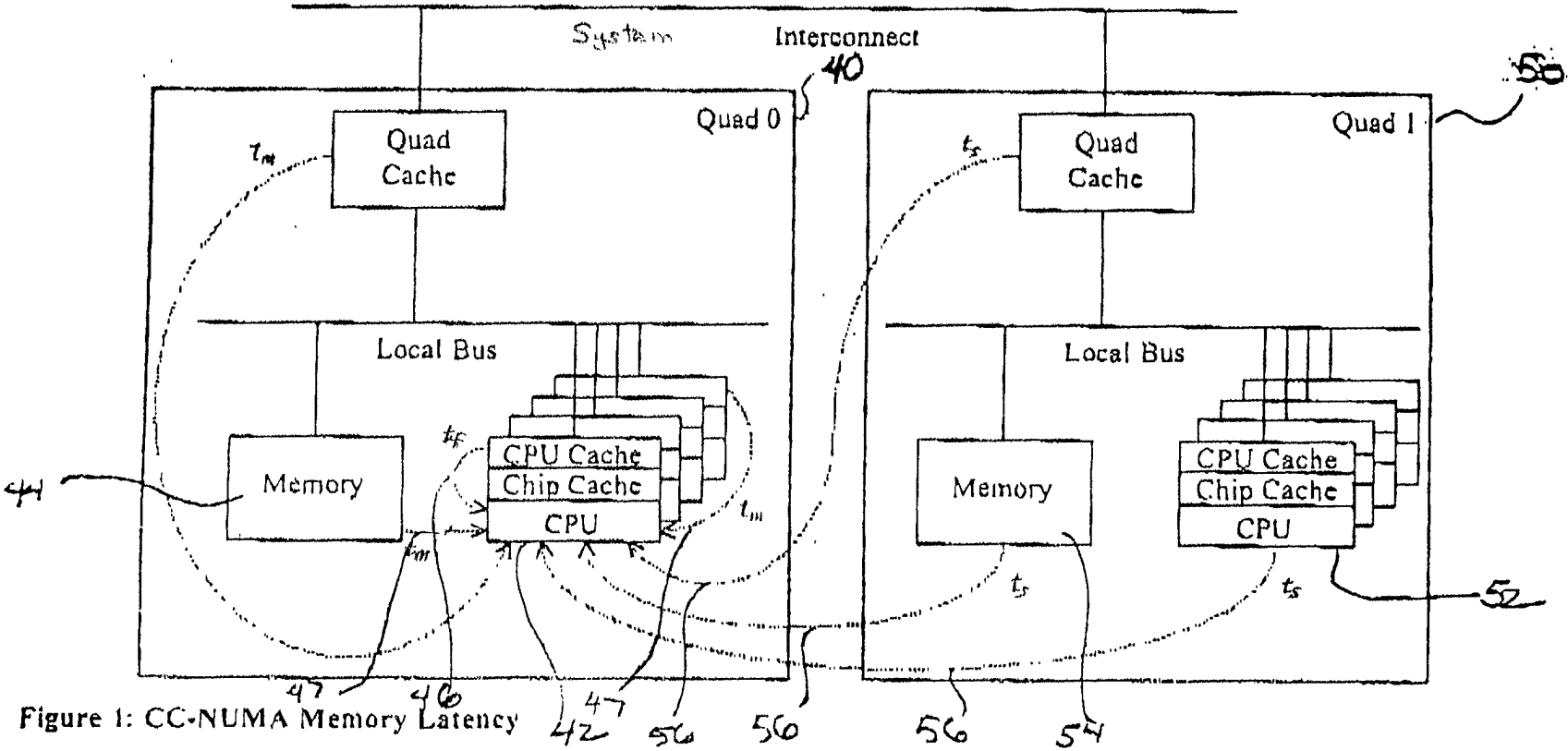


Figure 1: CC-NUMA Memory Latency

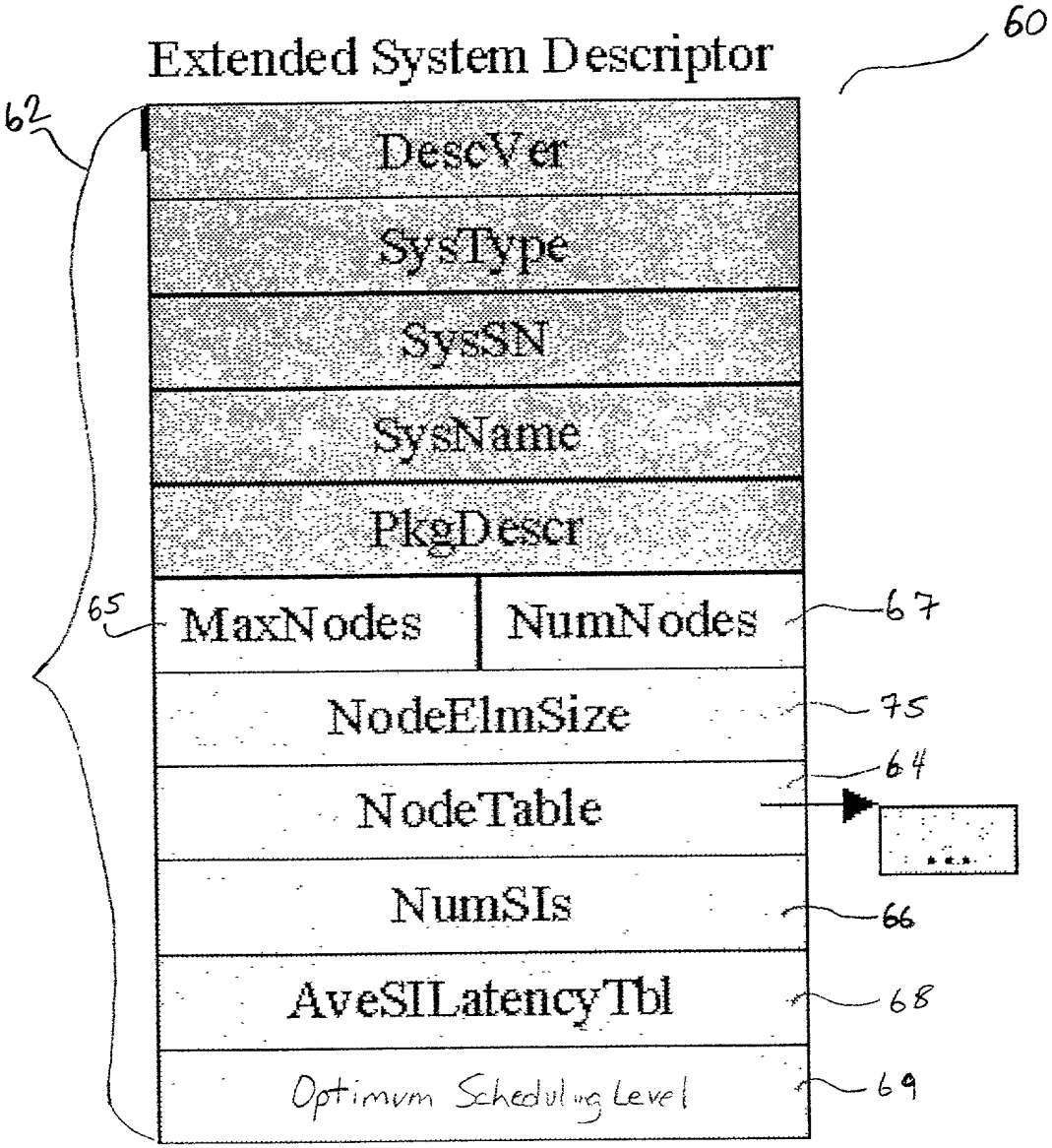
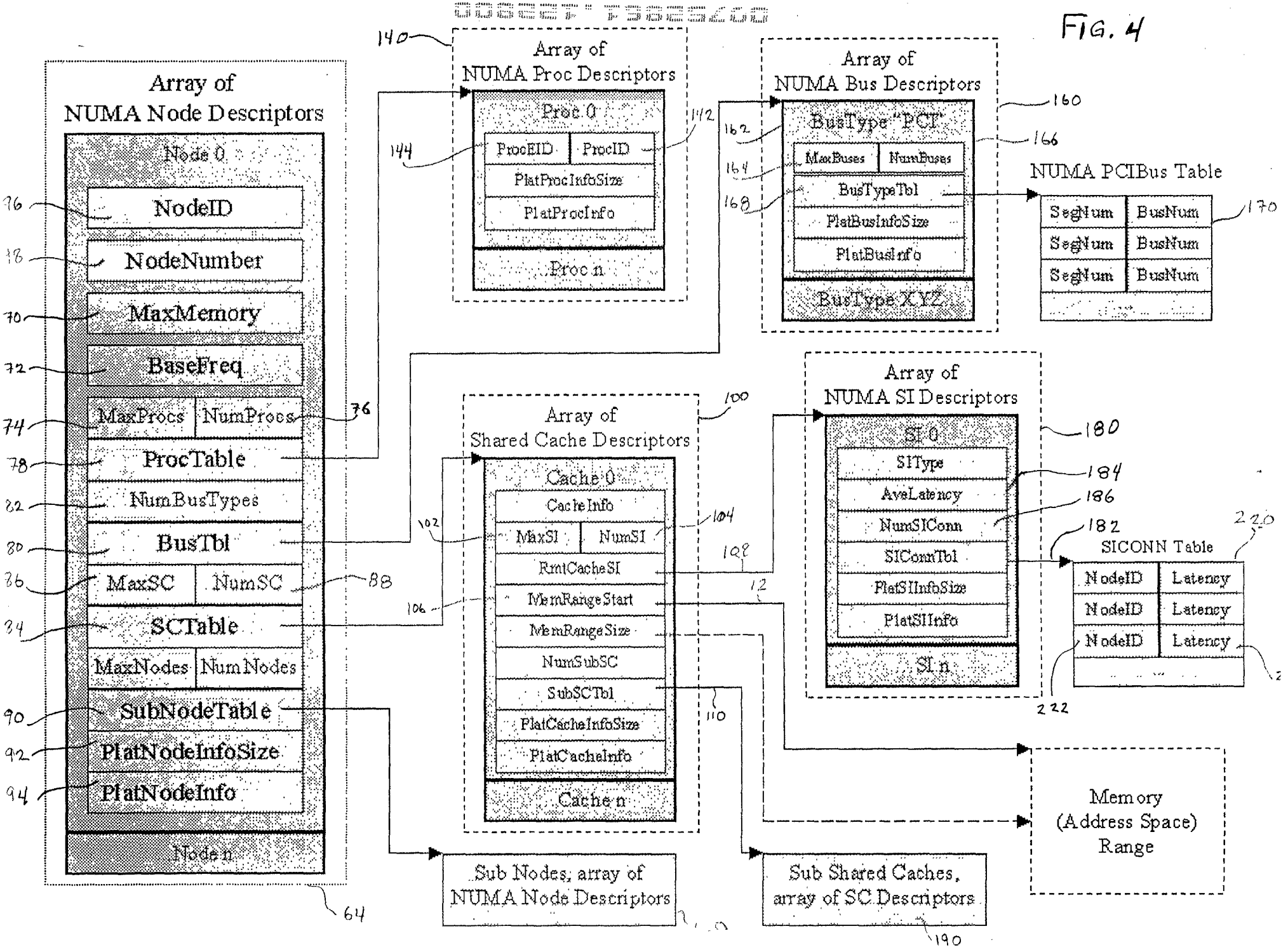

Extended System Descriptor
60
62
DescVer
SysType
SysSN
SysName
PkgDescr
65
MaxNodes
NumNodes
67
NodeElmSize
75
64
NodeTable
NumSIs
66
AveSILatencyTbl
68
Optimum Scheduling Level
69

FIG. 3

FIG. 4


Array of
NUMA Node Descriptors
Node 0
NodeID
NodeNumber
MaxMemory
BaseFreq
MaxProcs
NumProcs
ProcTable
NumBusTypes
BusTbl
MaxSC
NumSC
SCTable
MaxNodes
NumNodes
SubNodeTable
PlatNodeInfoSize
PlatNodeInfo
Node n
64
96
98
70
72
74
76
78
82
80
86
88
84
90
92
94
Array of
NUMA Proc Descriptors
140
Proc 0
ProcEID
ProcID
PlatProcInfoSize
PlatProcInfo
Proc n
142
144
Array of
NUMA Bus Descriptors
160
BusType "PCI"
MaxBuses
NumBuses
BusTypeTbl
PlatBusInfoSize
PlatBusInfo
BusType XYZ
162
164
166
168
NUMA PCIBus Table
SegNum
BusNum
170
Array of
Shared Cache Descriptors
100
Cache 0
CacheInfo
MaxSI
NumSI
RmtCacheSI
MemRangeStart
MemRangeSize
NumSubSC
SubSCTbl
PlatCacheInfoSize
PlatCacheInfo
Cache n
102
104
106
108
110
Array of
NUMA SI Descriptors
180
SI 0
SIType
AveLatency
NumSIConn
SIConnTbl
PlatSIInfoSize
PlatSIInfo
SI n
184
186
182
220
SICONN Table
NodeID
Latency
222
112
Sub Nodes, array of
NUMA Node Descriptors
Sub Shared Caches,
array of SC Descriptors
190
Memory
(Address Space)
Range

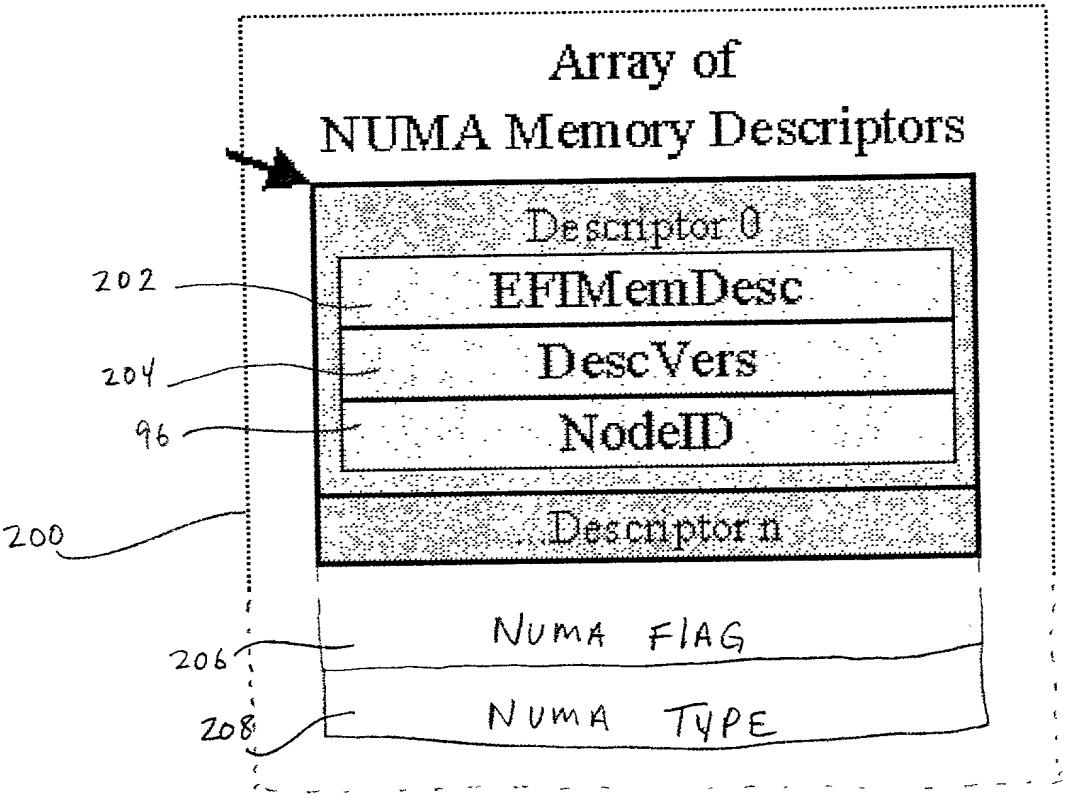
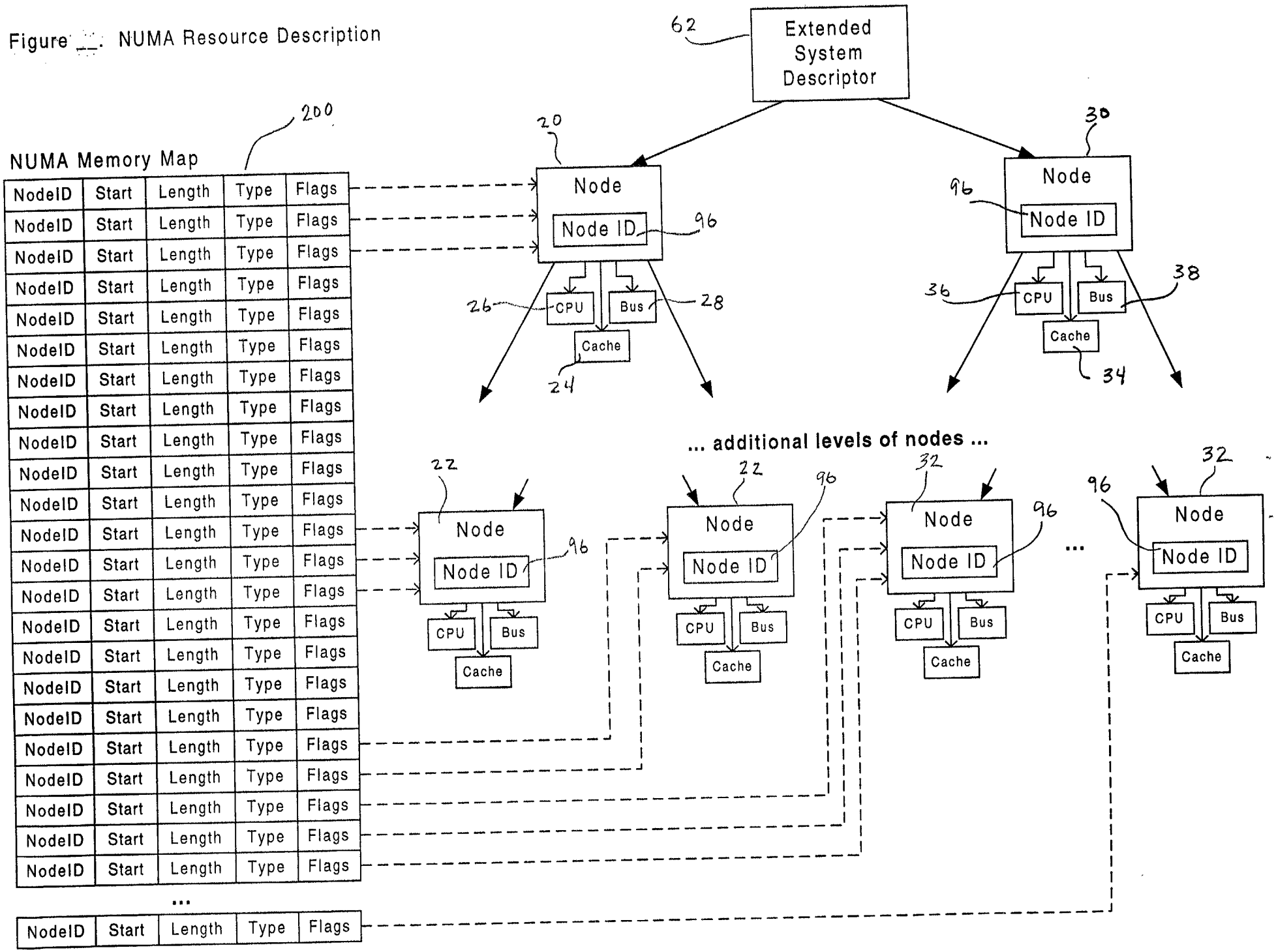

Array of
NUMA Memory Descriptors
Descriptor 0
EFIMemDesc
DescVers
NodeID
Descriptor n
NUMA FLAG
NUMA TYPE
202
204
96
200
206
208

FIG. 5

FIG. 6

Figure __: NUMA Resource Description



Example Resource Access Costing using NUMA Resource Description data structures

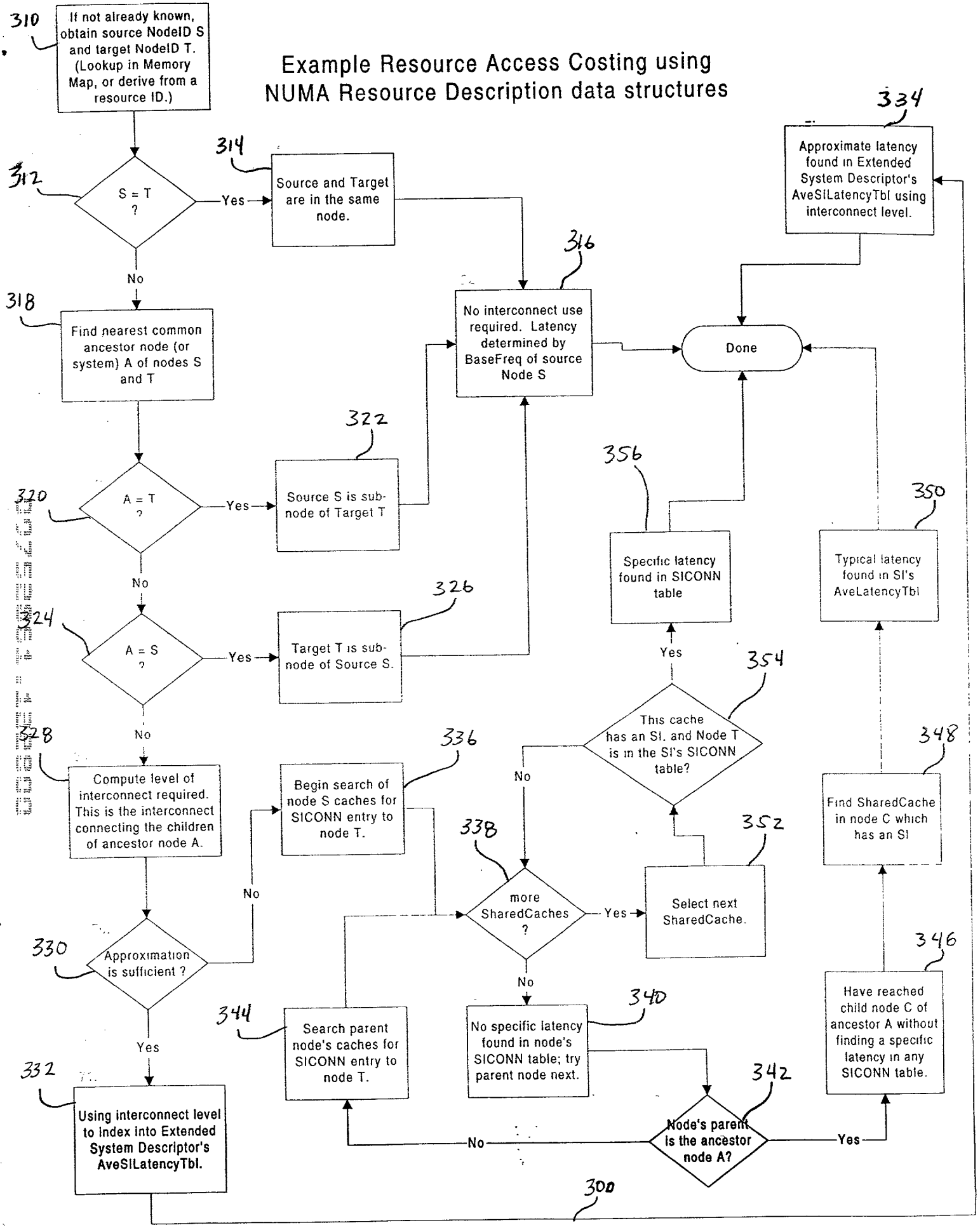


FIG. 7